Weltrend

DESCRIPTION

The WT8048 is a 8 pin P-DIP package IC, designed for the application of Power Saving Monitor or Green Monitor.

As per DPMS proposal, the WT8048 provides a detective circuit of monitor power management for the convenience of designers in designing Power Saving Monitor.

FEATURES

{   Accepting two seperated H&V synchronous signals with positive/ negative polarity.

{   Capable of processing horizontal frequency between 0Hz to 100kHz, and vertical frequency between 0Hz to 100Hz.

{   Power Saving mode - It can detect the conditions of monitor to decide which will be selected as following: ON mode / STAND_BY mode / SUSPEND mode / OFF mode.

{   An Override mode is defined to override the DPMS function during the design, test, burn-in manufacture or diagnostic process if desired.

APPLICATION

{   DPMS mode's detection for Green Monitor

E-Tech Electronics Ltd.

ORDERING INFORMATION

Part No.	Package	Description
WT8048	P-DIP 8L	OSC with 32768Hz Crystal
WT8048N1	P-DIP 8L	1. OSC with external resistor 2. With mute function
WT8048N2	P-DIP 8L	1. OSC with external resistor 2. Without mute function
*WT8048N3	P-DIP 8L	1. OSC with 3.58MHz resonator 2. With mute function
*WT8048N4	P-DIP 8L	1. OSC with 3.58MHz resonator 2. Without mute function

Note: "*" means "not available".

PIN CONFIGURATION

WT8048N1 / N3

HIN	1	8	VDD
VIN	2	7	OFF
OSC	3	6	STD_BY + SUSPEND
VSS	4	5	MUTE

WT8048 / N2 / N4

HIN	1	8	VDD
VIN	2	7	OFF
OSC	3	6	SUSPEND
VSS	4	5	STD_BY
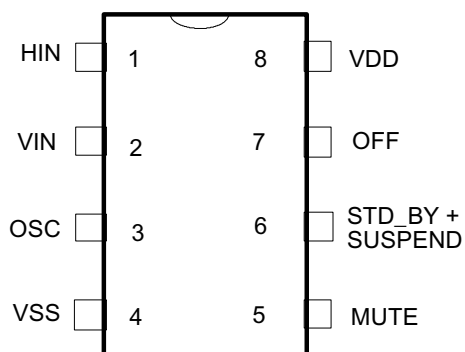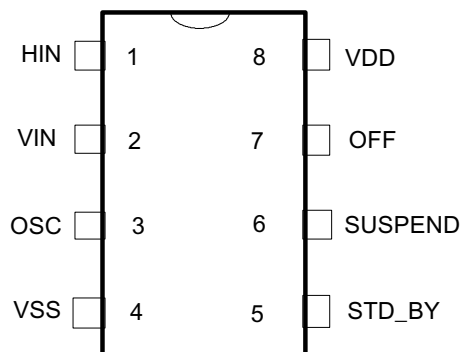
ABSOLUTE MAXIMUM RATING

ITEM	SYMBOL	VALUE	UNIT
Digital Supply Voltage	V_{DD}	5.5	V
Horizontal Sync. Input Voltage	V_{HS}	$V_{DD}(5)+0.3$	V_{PP}
Vertical Sync. Input Voltage	V_{VS}	$V_{DD}(5)+0.3$	V_{PP}
Power dissipation	P_D	30	mW
Operating Temperature Range	T_{OPT}	0 70	J
Storage Temperature Range	T_{STG}	-40 125	J

RECOMMENDED OPERATING CONDITIONS

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Digital Supply Voltage	$V_{DD}(5)$	4.5	5	5.5	V
Supply Current (Stand-by)	I_P			1	mA
Synchronous Input Voltage Low	V_{IL}			0.8	V_{PP}
Synchronous Input Voltage High	V_{IH}	2.4	4	5.5	V_{PP}

ELECTRICAL CHARACTERISTICS

A. WT8048

(V_{DD}=5V, T_{OPT}=24 ʃ F_{OSC}=32768Hz)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input Current (H_{IN}, V_{IN}), when V_{IN}=5V	I_{IN1}			5	μA
Open Drain Output Low, when I_{OL} = 6mA	V_{OL}			0.4	V_{PP}
Open Drain Sink Current, when V_{OL} = 0.4V	V_{OL}			6	mA
Input Current (OSC), when V_{IN} = 5V	I_{IN3}			5	μA

B. WT8048N1 / N2

(V_{DD}=5V, T_{OPT}=24 ʃ F_{OSC}= 450KHz)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input Current (H_{IN}, V_{IN}), when V_{IN}=5V	I_{IN1}			5	μA
Open Drain Output Low, when I_{OL} = 6mA	V_{OL}			0.4	V_{PP}
Open Drain Sink Current, when V_{OL} = 0.4V	V_{OL}			6	mA
Input Current (OSC), when V_{IN} = 5V	I_{IN3}			15	mA

C. WT8048N3 / N4

(V_{DD}=5V, T_{OPT}=24 ʃ F_{OSC}= 3.58MHz)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input Current (H_{IN}, V_{IN}), when V_{IN}=5V	I_{IN1}			5	μA
Open Drain Output Low, when I_{OL} = 6mA	V_{OL}			0.4	V_{PP}
Open Drain Sink Current, when V_{OL} = 0.4V	V_{OL}			6	mA
Input Current (OSC), when V_{IN} = 5V	I_{IN3}			5	μA

PIN DESCRIPTION

Pin No.		Name	Function	Structure of Terminal
WT8048N1/N3	WT8048/N2/N4			
1	1	H_{SIN}	Input terminal of horizontal synchronous signal	Input, TTL compatible
2	2	V_{SIN}	Input terminal of vertical synchronous signal	Input, TTL compatible
3	3	OSC	A clock generator circuit is built into the chip. So, if a resonator is connected to OSC pin and ground, a clock signal can be obtained.	Input
4	4	V_{SS}	Ground	
	5	STD_BY	Indicate in Stand_By mode	Output, open drain
5		Mute	Indicate in Mute mode	
	6	Suspend	Indicate in Suspend mode	Output, open drain
6		Suspend + STD_BY	Indicate in Suspend and stand_By mode	
7	7	Off	Indicate in Off mode	Output, open drain
8	8	V_{DD}	5 volts power supply	

APPLICATION DESCRIPTION

DPMS (Display Power Management Signaling) Dection

As per DPMS proposal WT8048 provides Monitor Power Management Detection Circuit for the convenience of monitor designers in designing power saving minitors, or the so called "Green Monitors". Please refer to the table 1 as below for power states defined in the DPMS.

DPMS requires at least 5 seconds delay before transition from ON state to any power saving state, to avoid unintentionally entering a power saving state during display resoultion changes and timing mode changes. And it can be done instaneously, for the transition between any power saving state.

Table 1 Display Power Management Summary

State	Signals			DPMS Compliance Requirement	Power Savings	Recovery Time
	Horizontal	Vertical	Video			
On	Pulse	Pulses	Active	Mandatory	None	Not Applicable
Stand-By	No Pulses	Pulses	Blanked	Optional	Minimal	Short
Suspend	Pulse	No Pulses	Blanked	Mandatory	Substantial	Longer
Off	No Pulses	No Pulses	Blanked	Mandatory	Maximum	System Dependent

* "No Pulse" represents the frequency of Hsin or Vsin less than or equal to 10Hz, but "Pulses" represents that frequency of Hsin greater than or equal to 15KHz (WT8048), 10KHz (WT8048N1 / N2 / N3 / N4) and Vsin greater than or equal to 40Hz.

The Way WT8048 implements VESA DPMS

As shown on Table 2, when H_SYNC / V_SYNC signals transition from ON state to any one of the three power saving state, WT8048 will delay 5.9 seconds to meet the VESA DPMS requirement: the minimum 5 seconds delay to avoid unintentionally entering a power saving state during display resolution and timing mode changes. If during this delay time period, H_SYN and V_SYN signals return to ON state, then all three power management pins will remain ON state. If power management state of H_SYNC and V_SYNC prolong for more than 5.9 seconds, then these three power management pins will change to the corresponding states. While changing from any power saving state back to ON state will take about 0.368 second for H_SYNC / V_SYNC pulse checking. And transition between any power saving state will be done immediately.

Table 2: The truth table of Power Saving Detector

MODE	H_{SIN}	V_{SIN}	STD_BY	SUSPEND	OFF
ON	Pulses	Pulses	1	1	1
STAND_BY	No Pulses	Pulses	0	1	1
SUSPEND	Pulses	No Pulses	0	0	1
OFF	No Pulses	No Pulses	0	0	0
OVERRIDE	No Pulses	No Pulses	1	1	1
	Manually Power On				

Synchronization Signals

The basis of DPMS standard is the condition of the synchronization signals to the display. Two conditions are defined: pulses and no pulses.

{ PULSES
   pulses for the Horizontal Sync. Signal are defined as greater than 10KHz repetition frequency and pulses for the Vertical Sync. Signal are defiened as greater than 40Hz repetition frequency.

{ NO PULSES
   No pulses is defined as less than 10Hz repetition frequency with less than 25% duty cycle

Please refer to the Fig. 1 for the way WT8048 Implement pulses/ no pulses state, between 10Hz and 15KHz / 10KHz, 10Hz and 40Hz. WT8048 use hystersis technique to stable state in between.
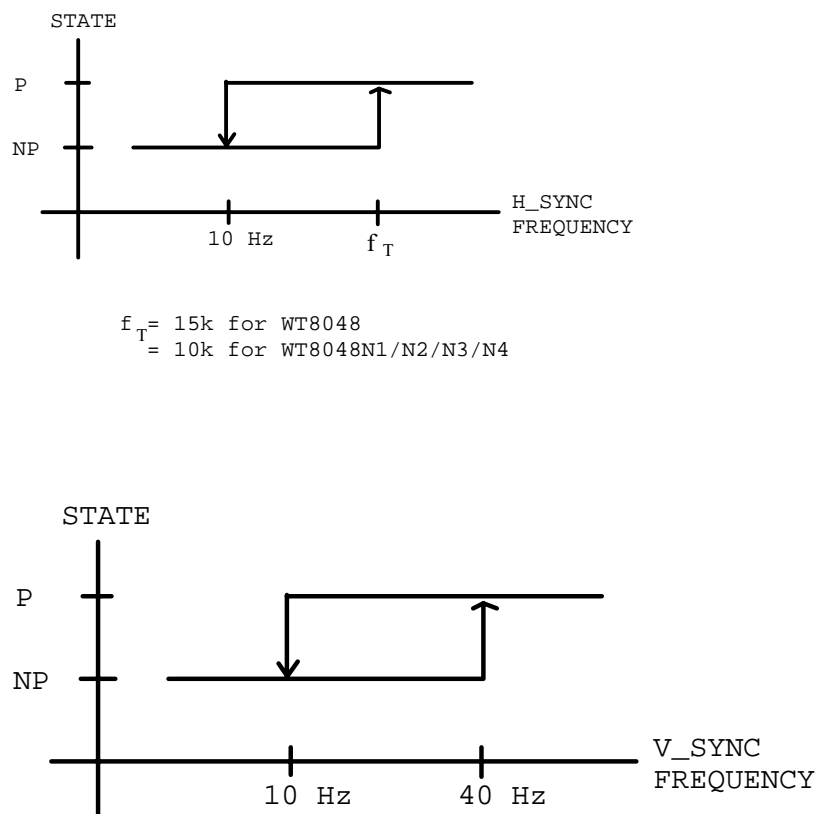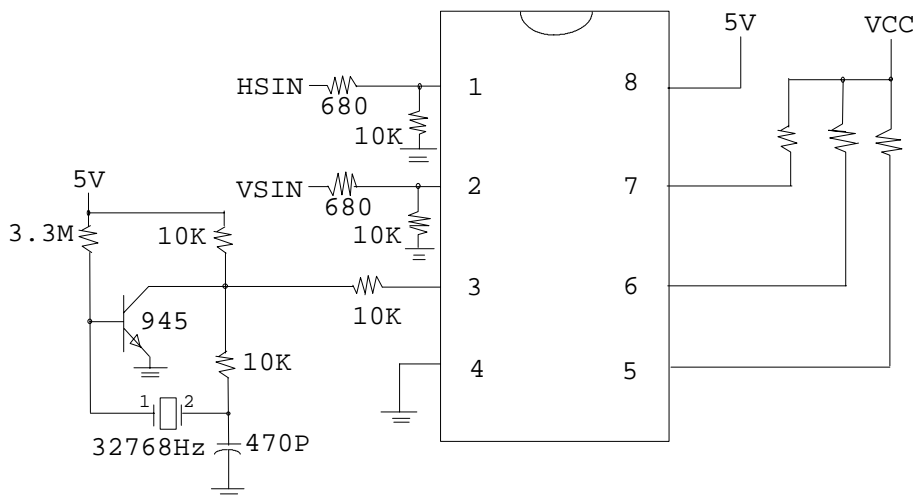

Figure 1: pulses / no pulses state implementation

OVERRIDE mode

To initiate Override, both the horizontal and vertical sync signals shall be in the no pulses condition when the display is manually powered on. This condition should be maintained during the entire time Override is required. As soon as pulses are detected on either horizontal or vertical sync signal. The display shall enter DPMS operation.

Three power management pins are open drain structure and active low. If you do not need all those three power saving states in your design. You can just short two or three pins of the pins: for example, by shorting pin STD_BY and pin Suspend, you will have only two power saving stated, that is OFF and Suspend states, so you have three states total, including ON state.
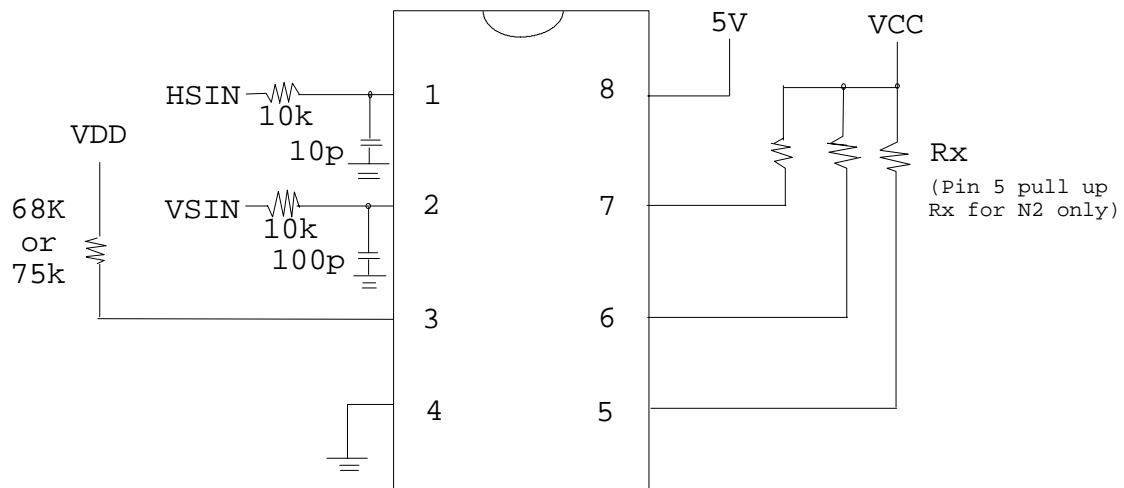
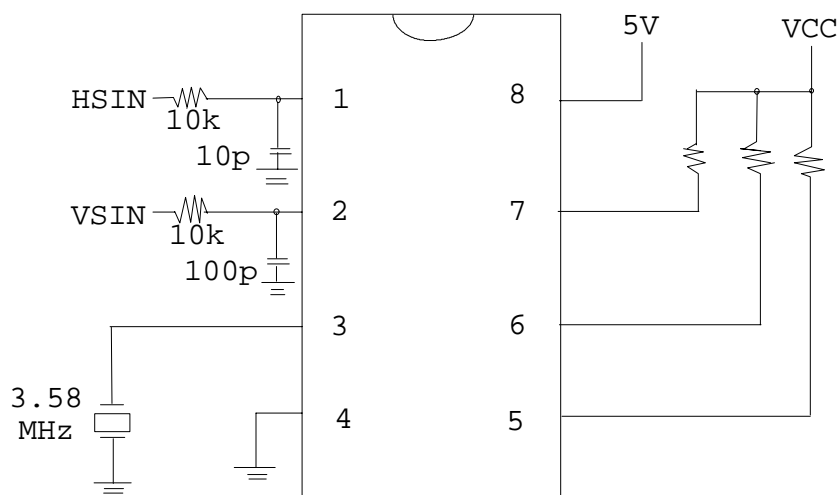## *TYPICAL APPLICATION CIRCUIT*

WT8048:

NOTE:

1. Transistor: 2SC945　A }300　 C
2. VDD: +5V ± 10%

WT8048N1 / N2:

HSIN —WW— 10k
10p
VDD
68K
or
75k
VSIN —WW— 10k
100p

1	8	5V	VCC
2	7		Rx
3	6		(Pin 5 pull up Rx for N2 only)
4	5		

NOTE: Connect pin 3 with single resistor for RC oscillation.

WT8048N3 / N4:

HSIN —WW— 10k
10p
VSIN —WW— 10k
100p

1	8	5V	VCC
2	7		
3	6		
4	5		

3.58
MHz

NOTE:

1.   Connect pin 3 with 3.58MHz resonator have good precision of delay time, frequency division point.
2.   This package is not available for production.