

GSS6982**DUAL N-CANNEL ENHANCEMENT MODE POWER MOSFET**

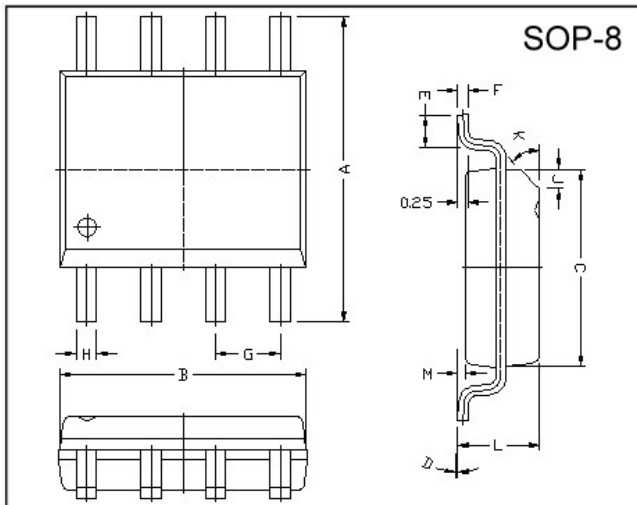
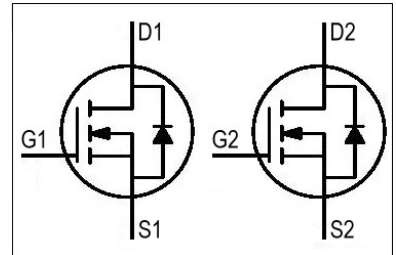
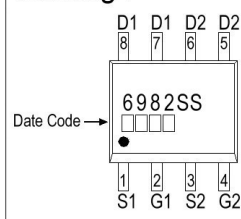
CH1	BVDSS	30V
	RDS(ON)	18mΩ
	ID	8.5A
CH2	BVDSS	30V
	RDS(ON)	26mΩ
	ID	7.3A

Description

The GSS6982 provide the designer with the best combination of fast switching, ruggedized device design, ultra low on-resistance and cost-effectiveness.

Features

- *Low On-resistance
- *Fast Switching

Package Dimensions**Marking :**

REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.80	6.20	M	0.10	0.25
B	4.80	5.00	H	0.35	0.49
C	3.80	4.00	L	1.35	1.75
D	0°	8°	J	0.375 REF.	
E	0.40	0.90	K	45°	
F	0.19	0.25	G	1.27 TYP.	

Absolute Maximum Ratings

Parameter	Symbol	Ratings		Unit
		CH-1	CH-2	
Drain-Source Voltage	V_{DS}	30	30	V
Gate-Source Voltage	V_{GS}	±25	±25	V
Continuous Drain Current ³	$I_D @ T_A=25^{\circ}C$	8.5	7.3	A
Continuous Drain Current ³	$I_D @ T_A=70^{\circ}C$	6.8	5.8	A
Pulsed Drain Current ¹	I_{DM}	30	30	A
Total Power Dissipation	$P_D @ T_A=25^{\circ}C$	2.0		W
Linear Derating Factor		0.016		W/°C
Operating Junction and Storage Temperature Range	T_j, T_{stg}	-55 ~ +150		°C

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-ambient ³ Max.	R_{thj-a}	62.5	°C/W

CH-1 Electrical Characteristics (T_j = 25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV _{DSS}	30	-	-	V	V _{GS} =0, I _D =250uA
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS} / \Delta T_j$	-	0.03	-	V/°C	Reference to 25°C, I _D =1mA
Gate Threshold Voltage	V _{GS(th)}	1.0	-	3.0	V	V _{DS} =V _{GS} , I _D =250uA
Forward Transconductance	g _{fs}	-	12	-	S	V _{DS} =10V, I _D =8A
Gate-Source Leakage Current	I _{GSS}	-	-	±100	nA	V _{GS} = ±25V
Drain-Source Leakage Current(T _j =25°C)	I _{DSS}	-	-	1	uA	V _{DS} =30V, V _{GS} =0
Drain-Source Leakage Current(T _j =70°C)		-	-	25	uA	V _{DS} =24V, V _{GS} =0
Static Drain-Source On-Resistance ²	R _{DS(on)}	-	15	18	mΩ	V _{GS} =10V, I _D =8A
		-	23	30		V _{GS} =4.5V, I _D =6A
Total Gate Charge ²	Q _g	-	14	22	nC	I _D =8A
Gate-Source Charge	Q _{gs}	-	4	-		V _{DS} =24V
Gate-Drain ("Miller") Charge	Q _{gd}	-	8	-		V _{GS} =4.5V
Turn-on Delay Time ²	T _{d(on)}	-	12	-	ns	V _{DS} =15V
Rise Time	T _r	-	7	-		I _D =1A
Turn-off Delay Time	T _{d(off)}	-	25	-		V _{GS} =10
Fall Time	T _f	-	9	-		R _G =3.3Ω R _D =15Ω
Input Capacitance	C _{iss}	-	1050	1680	pF	V _{GS} =0V
Output Capacitance	C _{oss}	-	240	-		V _{DS} =25V
Reverse Transfer Capacitance	C _{rss}	-	165	-		f=1.0MHz
Gate Resistance	R _g	-	1.6	2.4	Ω	f=1.0MHz

Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Forward On Voltage ²	V _{SD}	-	-	1.2	V	I _S =1.7A, V _{GS} =0V
Reverse Recovery Time ²	T _{rr}	-	23	-	ns	I _S =8A, V _{GS} =0V
Reverse Recovery Charge	Q _{rr}	-	15	-	nC	dI/dt=100A/μs

Notes: 1. Pulse width limited by Max. junction temperature.

2. Pulse width ≤ 300us, duty cycle ≤ 2%.

3. Surface mounted on 1 in² copper pad of FR4 board, t ≤ 10sec; 135°C/W when mounted on Min. copper pad.

CH-2 Electrical Characteristics (T_j = 25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV _{DSS}	30	-	-	V	V _{GS} =0, I _D =250uA
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS} / \Delta T_j$	-	0.03	-	V/°C	Reference to 25°C, I _D =1mA
Gate Threshold Voltage	V _{GS(th)}	1.0	-	3.0	V	V _{DS} =V _{GS} , I _D =250uA
Forward Transconductance	g _{fs}	-	10	-	S	V _{DS} =10V, I _D =7A
Gate-Source Leakage Current	I _{GSS}	-	-	±100	nA	V _{GS} = ±25V
Drain-Source Leakage Current(T _j =25°C)	I _{DSS}	-	-	1	uA	V _{DS} =30V, V _{GS} =0
Drain-Source Leakage Current(T _j =70°C)		-	-	25	uA	V _{DS} =24V, V _{GS} =0
Static Drain-Source On-Resistance ²	R _{DS(on)}	-	22	26	mΩ	V _{GS} =10V, I _D =7A
		-	36	45		V _{GS} =4.5V, I _D =5A
Total Gate Charge ²	Q _g	-	9	15	nC	I _D =7A
Gate-Source Charge	Q _{gs}	-	3	-		V _{DS} =24V
Gate-Drain ("Miller") Charge	Q _{gd}	-	5	-		V _{GS} =4.5V
Turn-on Delay Time ²	T _{d(on)}	-	9	-	ns	V _{DS} =15V
Rise Time	T _r	-	6	-		I _D =1A
Turn-off Delay Time	T _{d(off)}	-	19	-		V _{GS} =10
Fall Time	T _f	-	6	-		R _G =3.3Ω R _D =15Ω
Input Capacitance	C _{iss}	-	640	1030	pF	V _{GS} =0V
Output Capacitance	C _{oss}	-	150	-		V _{DS} =25V
Reverse Transfer Capacitance	C _{rss}	-	105	-		f=1.0MHz
Gate Resistance	R _g	-	1.7	2.5	Ω	f=1.0MHz

Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Forward On Voltage ²	V _{SD}	-	-	1.2	V	I _S =1.7A, V _{GS} =0V
Reverse Recovery Time ²	T _{rr}	-	18	-	ns	I _S =7A, V _{GS} =0V
Reverse Recovery Charge	Q _{rr}	-	8	-	nC	di/dt=100A/μs

Notes: 1. Pulse width limited by Max. junction temperature.

2. Pulse width ≤ 300us, duty cycle ≤ 2%.

3. Surface mounted on 1 in² copper pad of FR4 board, t ≤ 10sec; 135°C/W when mounted on Min. copper pad.

Characteristics Curve CH-1

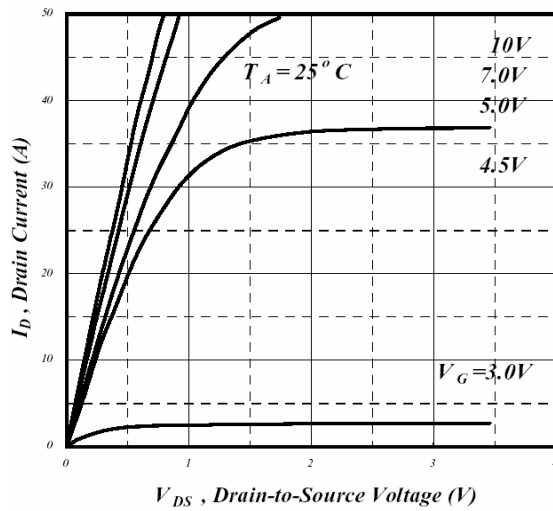


Fig 1. Typical Output Characteristics

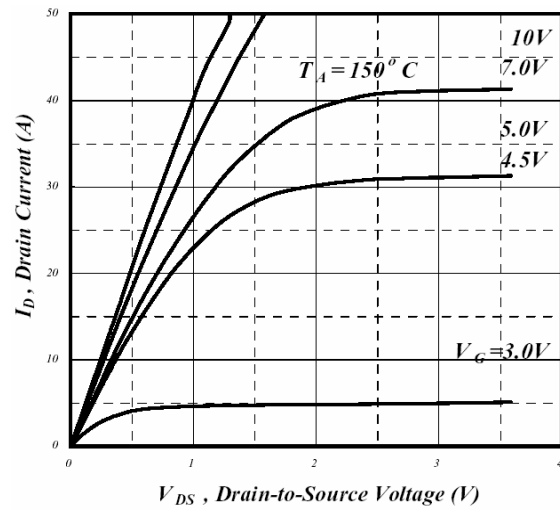


Fig 2. Typical Output Characteristics

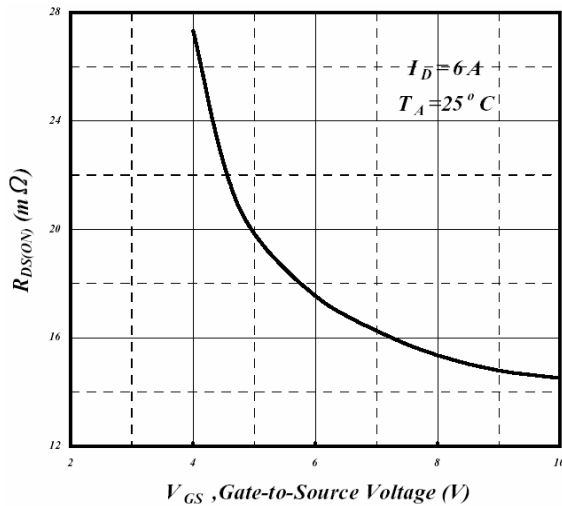


Fig 3. On-Resistance v.s. Gate Voltage

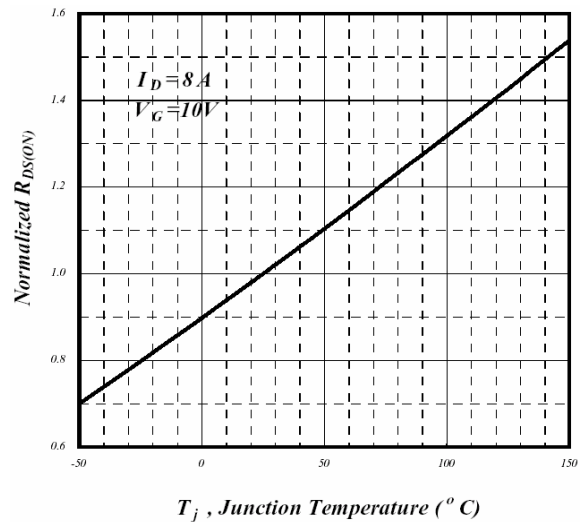


Fig 4. Normalized On-Resistance v.s. Junction Temperature

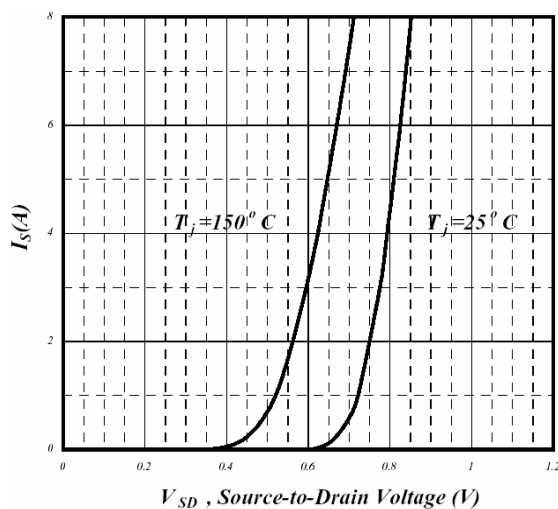


Fig 5. Forward Characteristics of Reverse Diode

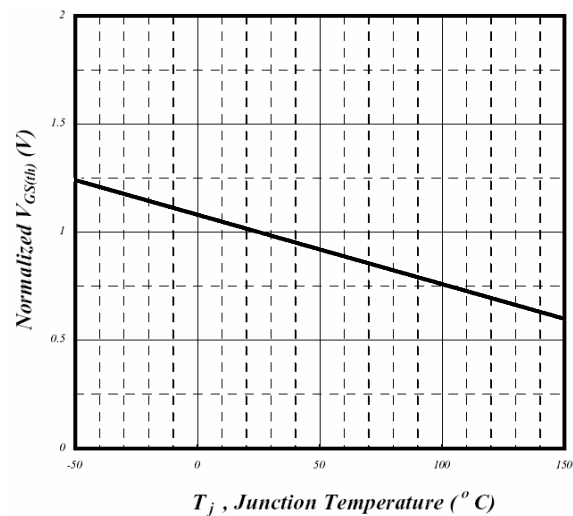


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

CH-1

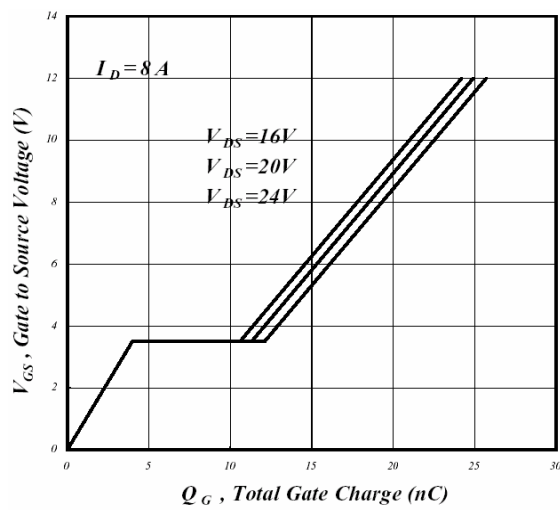


Fig 7. Gate Charge Characteristics

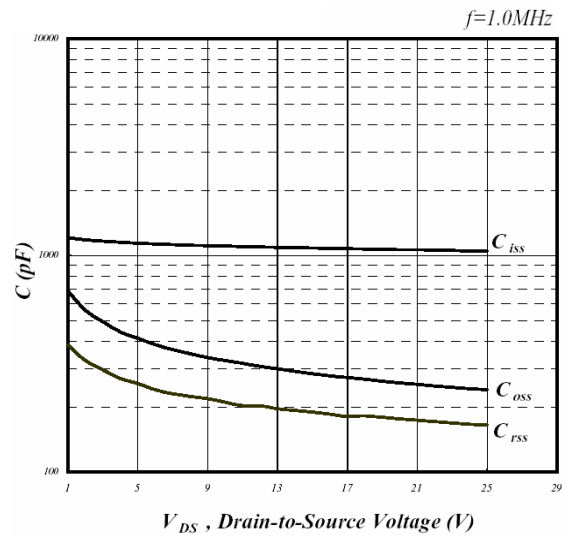


Fig 8. Typical Capacitance Characteristics

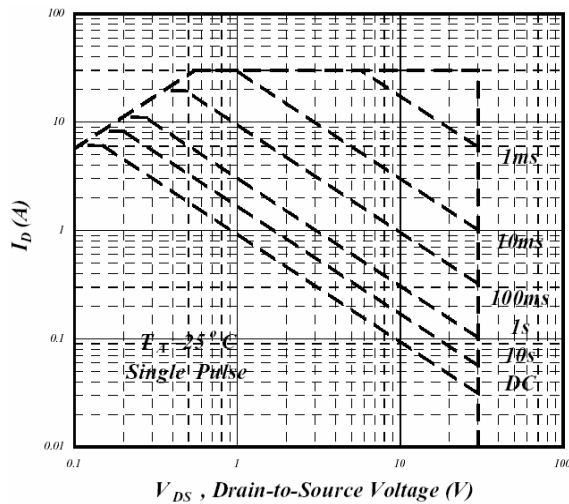


Fig 9. Maximum Safe Operating Area

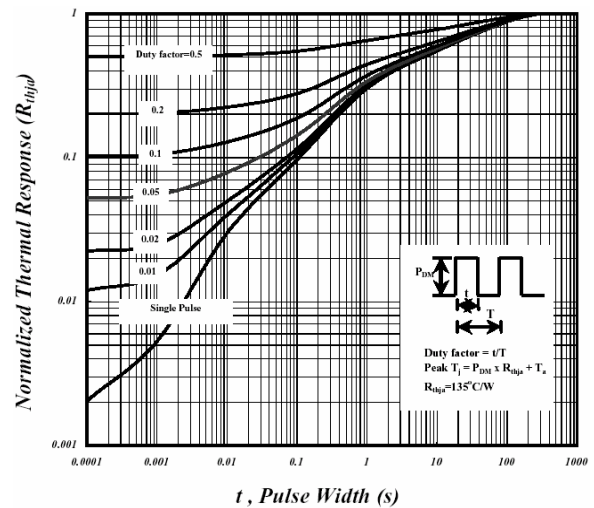


Fig 10. Effective Transient Thermal Impedance

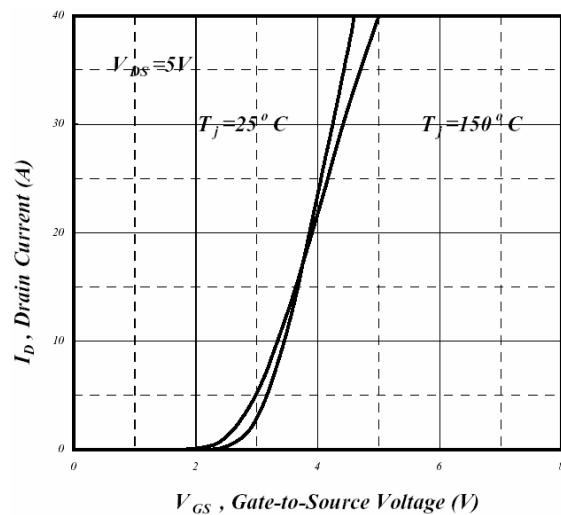


Fig 11. Transfer Characteristics

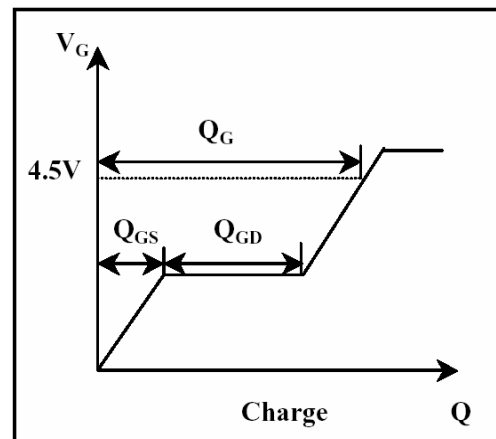


Fig 12. Gate Charge Waveform

CH-2

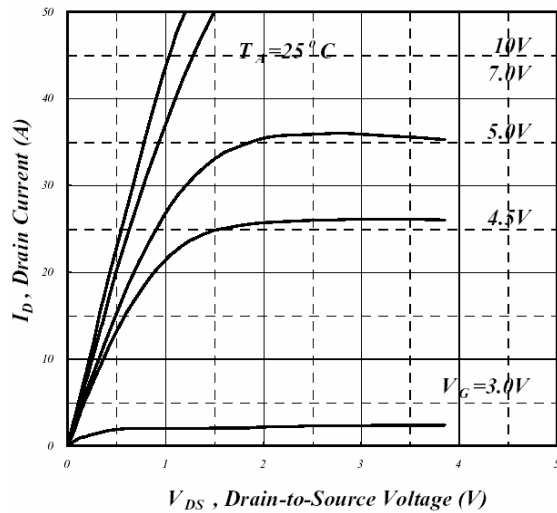


Fig 1. Typical Output Characteristics

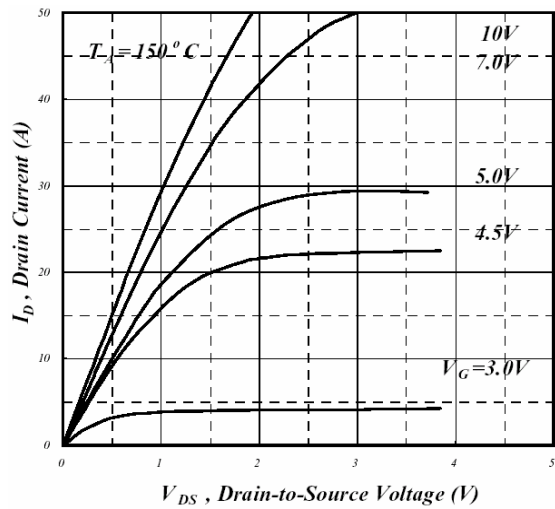


Fig 2. Typical Output Characteristics

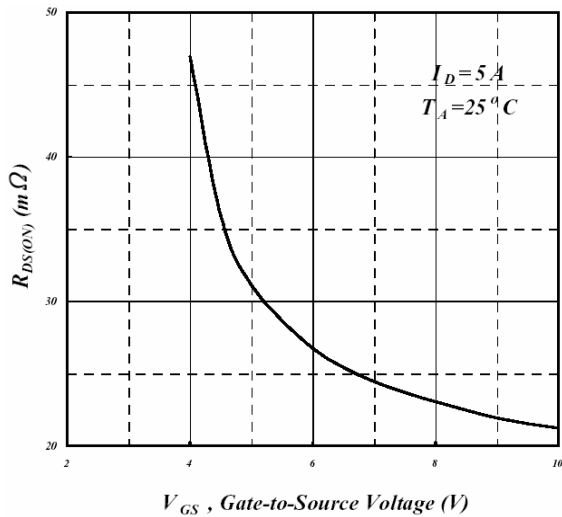


Fig 3. On-Resistance v.s. Gate Voltage

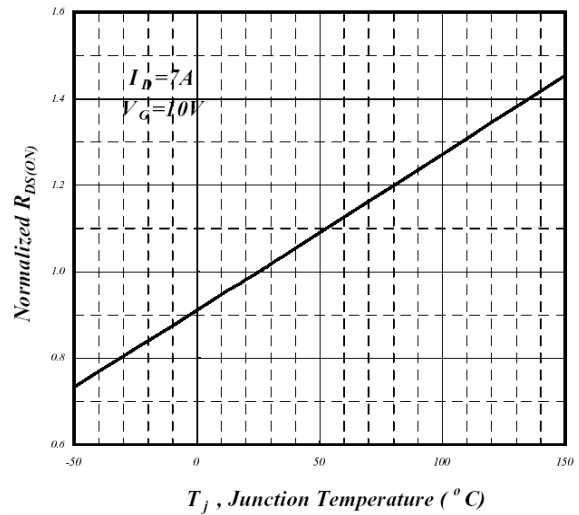


Fig 4. Normalized On-Resistance v.s. Junction Temperature

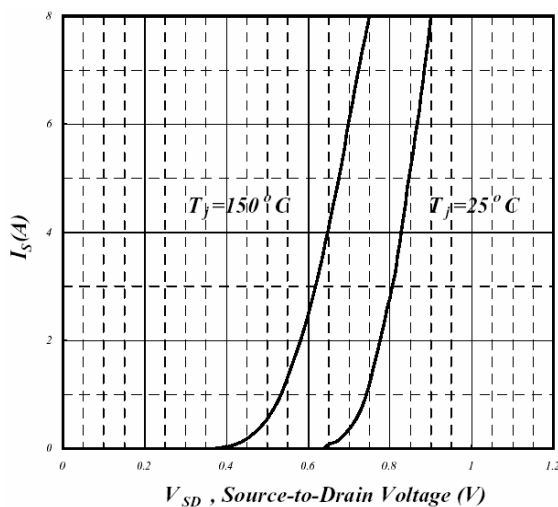


Fig 5. Forward Characteristics of Reverse Diode

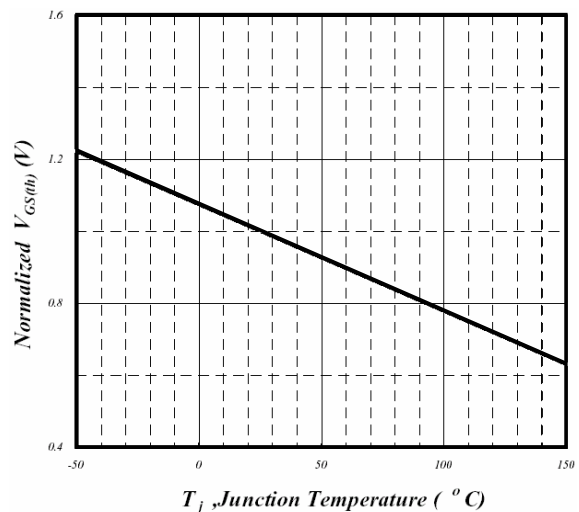


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

CH-2

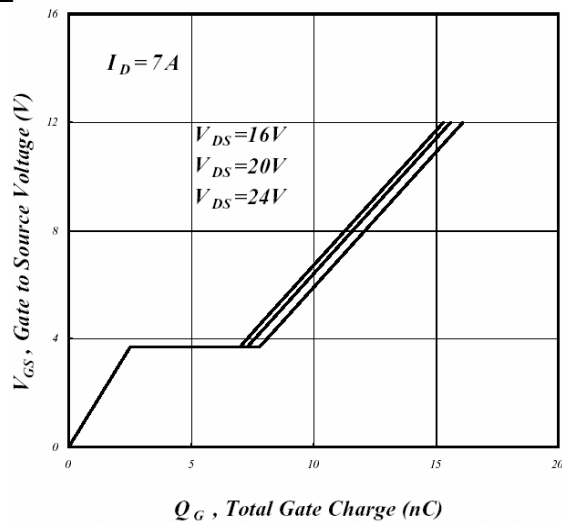


Fig 7. Gate Charge Characteristics

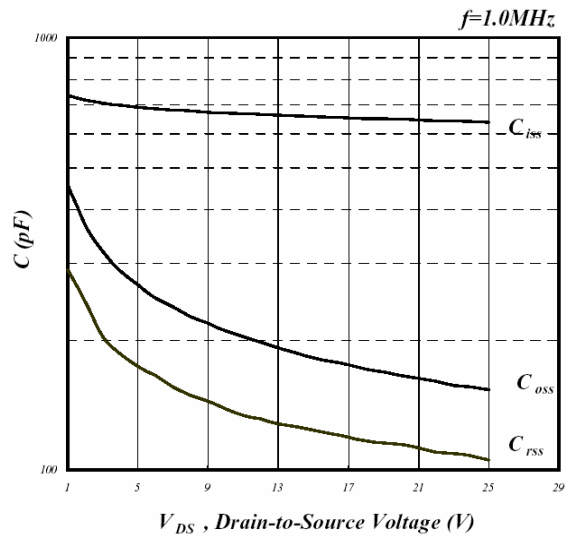


Fig 8. Typical Capacitance Characteristics

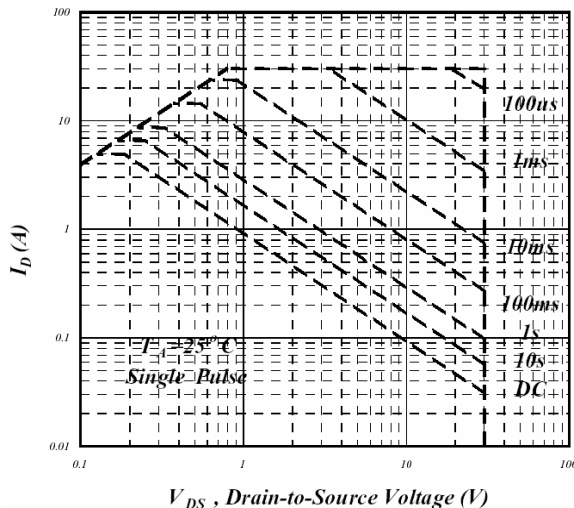


Fig 9. Maximum Safe Operating Area

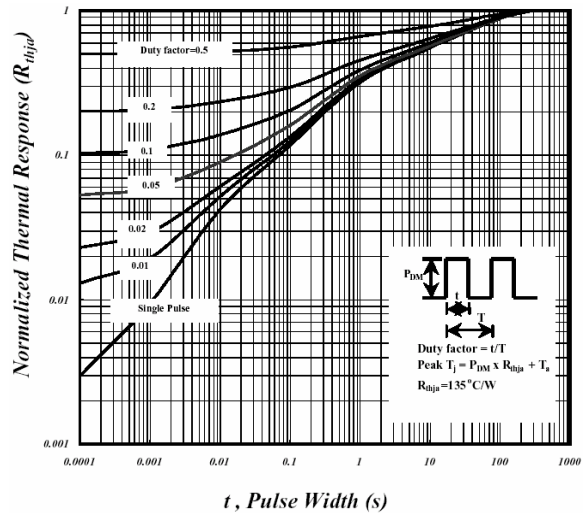


Fig 10. Effective Transient Thermal Impedance

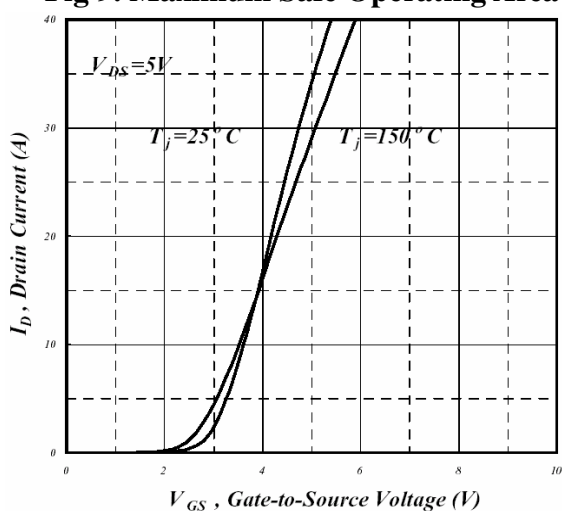


Fig 11. Transfer Characteristics

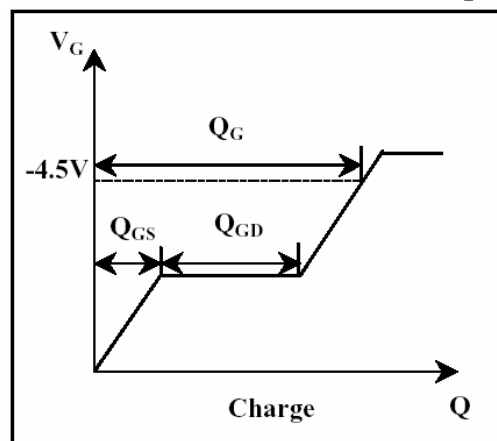


Fig 12. Gate Charge Waveform

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