

GP3843

HIGH PERFORMANCE CURRENT MODE CONTROLERS

Description

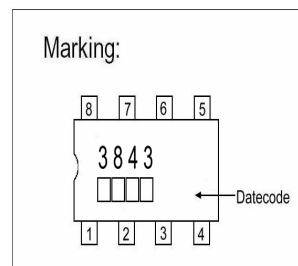
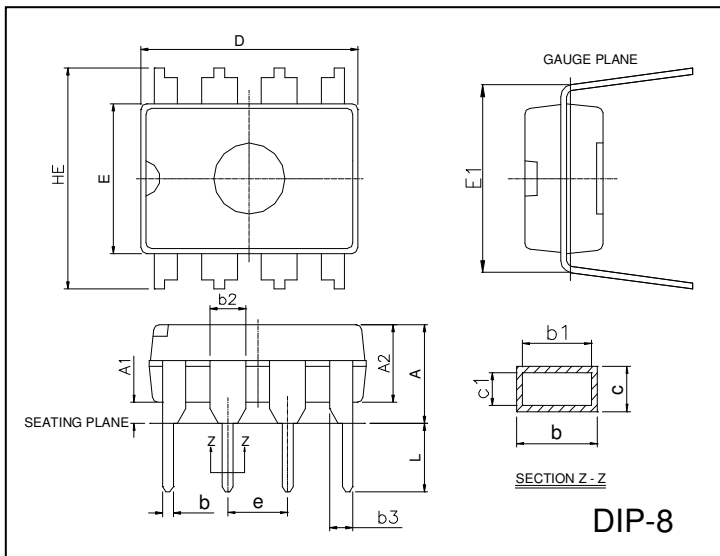
The GP3843 is specifically designed for Off-Line and dc-to-dc converter applications offering the designer a cost-effective solution with minimal external components.

The GP3843 has UVLO thresholds 8.5V(on) and 7.6V(off), ideally suited for off-line converters.

Features

- *Trimmed Oscillator for Precise Frequency Control
- *Oscillator Frequency Guaranteed at 250kHz
- *Current Mode Operation to 500kHz
- *Automatic Feed Forward Compensation
- *latching PWM for Cycle-By-Cycle Current Limiting
- *Internally Trimmed Reference with Undervoltage Lockout
- *High Current Totem Pole Output
- *Undervoltage Lockout with Hysteresis
- *Low Startup and Operating Current

Package Dimensions



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	-	0.5334	c1	0.203	0.279
A1	0.381	-	D	9.017	10.16
A2	2.921	4.953	E	6.096	7.112
b	0.356	0.559	E1	7.620	8.255
b1	0.356	0.508	e	2.540 BSC	
b2	1.143	1.778	HE	-	10.92
b3	0.762	1.143	L	2.921	3.810
c	0.203	0.356			

DIP-8L	Function	Description
	Pin1: Compensation	This pin is the Error Amplifier output and is made available for loop compensation.
	Pin2: Voltage Feedback	This is the inverting input of the Error Amplifier. It's normally connected to the Switching power supply output through a resistor divider.
	Pin3: Current Sense	A voltage proportional to inductor current is connected to this input .The PWM uses this information to terminate the output switch conduction.
	Pin4: RT/CT	The oscillator frequency and maximum output duty cycle are programmed by connecting resistor RT to Vref and capacitor CT to ground .Operation 500kHz is possible.
	Pin5: Ground	This pin is the combined control circuitry and power ground.
	Pin6: Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1 A are sourced and sunk by this pin.
	Pin7: Vcc	This pin is the positive supply of the control IC.
	Pin8: Vref	This is the reference output .It provides charging current for capacitor CT through resistor RT.

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	VALUE	Unit
Total power Supply and Zener current	(ICC+Iz)	30	mA
Output current, source or sink(note1)	Io	1.0	A
Output energy(capacitive load per cycle)	W	5.0	μJ
Current sense and voltage feedback inputs	Vin	-0.3 to 5.5	V

Error Amplifier Output Sink Current	I _o	10	mA
Power Dissipation at Thermal Characteristics	PD P _{θJA}	1250 100	mW °C/W
Storage Temperature Range	T _{stg}	-65 to 150	°C
Operating Junction Temperature	T _J	+150	°C
Operating ambient Temperature	T _A	0~+70	°C

Electrical Characteristics (0°C≤T_A≤70°C, V_{CC}=15V[note 2], R_T=10k, C_T=3.3nF, unless otherwise specified)

Parameter	SYMBOL	Test Conditions		Typ.	Max.	Unit
Reference Section						
Output Voltage	V _{REF}	T _J =25°C, I _o =1mA	4.90	5	5.1	V
Line Regulation	Reg _{line}	V _{CC} =12V to 25V		2.0	20	mV
Load Regulation	Reg _{load}	I _o =1mA to 20mA		3.0	25	mV
Temperature Stability	T _s			0.2	-	mV/°C
Total Output Variation	V _{REF}	Line, Load, Temperature	4.82	-	5.18	V
Output Noise Voltage	V _n	F=10kHz to 10Hz, T _J =25°C	-	50	-	μV
Long Term Stability	S	T _A =125°C, 1000Hrs	-	5	-	mV
Output Short Circuit current	I _{SC}		-30	-85	-180	mA

Oscillator Section

Frequency		T _J =25°C	49	52	55	KHz
		T _A =0°C to 70°C	48		56	
		T _J =25°C (R _T =6.2k, C _T =1.0nF)	225	250	275	
Frequency Change with Voltage	Δf _{osc} /ΔV	V _{CC} =12V to 25V		0.2	1.0	%
Frequency Change with Temperature	Δf _{osc} /ΔT	T _A = 0°C to 70 °C		0.5		%
Oscillator Voltage Swing(Peak to Peak)	V _{Osc}			1.6		V
Discharge Current	I _{dischg}	T _J =25°C	7.8	8.3	8.8	mA
		T _A = 0°C to 70°C	7.6		8.8	

Error Amplifier Section

Voltage Feedback Input	V _{FB}	V _o =2.5V	2.42	2.50	2.58	V
Input Bias Current	I _{IB}	V _{FB} =5.0V		-0.1	-2.0	μA
Open Loop Voltage Gain	A _{VOL}	V _o =2V to 4V	65	90		dB
Unity Gain Bandwidth	BW	T _J =25°C	0.7	1.0		MHz
Power Supply Rejection Ratio	PSRR	V _{CC} =12V to 25V	60	70		dB
Output Sink Current	I _{sink}	V _o =1.1V, V _{FB} =2.7V	2.0	12		mA
Output Source Current	I _{source}	V _o =5.0V, V _{FB} =2.3V	-0.5	-1.0		mA
Output Voltage Swing High State	V _{OH}	V _{FB} =2.3V, R _L =15K to GND	5.0	6.2		V
Output Voltage Swing Low State	V _{OL}	V _{FB} =2.7V, R _L =15K to V _{ref}		0.8	1.1	V

Current Sense section

Current Sense Input Voltage gain	A _v	(Note 3,4)	2.85	3.0	3.15	V/V
Maximum Current Sense Input Threshold	V _{th}	(Note 3)	0.9	1.0	1.1	V
Power Supply Rejection Ratio	PSRR	V _{CC} = 12 to 25V (Note 3)		70		dB
Input Bias Current	I _{IB}			-2	-10	μA
Propagation Delay	T _{plh} (in/out)	Current Sense Input to Output		150	300	ns
Output Low Voltage	V _{OL}	I _{sink} =20mA		0.1	0.4	V
		I _{sink} =200mA		1.6	2.2	V
Output High Level	V _{OH}	I _{source} =20mA	13	13.5		V
		I _{source} =200mA	12	13.4		V
Output Voltage with UVLO Activated	V _{OL}	V _{CC} =6.0V, I _{sink} =1.0mA		0.1	1.1	V
	(UVLO)					
Output Voltage Rise Time	t _r	T _J =25°C, C _L =1nF		50	150	ns
Output Voltage Fall Time	t _r	T _J =25°C, C _L =1nF		50	150	ns

Under-Voltage Lockout Section						
Startup Threshold	V _{th}		7.8	8.4	9.0	V
Min. Operating Voltage After Turn-on(V _{cc})	V _{OPR(min)}		7.0	7.6	8.2	V
PWM Section						
Maximum Duty Cycle	DC(MAX)		94	96		%
Minimum Duty Cycle	DC(MIN)				0	%
Total Device						
Power Startup Supply Current	I _{CC+IC}	V _{CC} =6.5V		0.2	0.3	mA
Power Operating Supply Current	I _{CC+IC}	Note 2		12	17	mA
Power Supply Zener Voltage	V _Z	I _{CC} =25mA	30	36		V

Note 1: Maximum Package power dissipation limits must be observed.

Note 2: Adjust V_{cc} above the Startup threshold before setting to 15V.

Note 3: This parameter is measured at the latch trip point with V_{FB}=0V.

Note 4: Comparator gain is defined as::

$$AV = \frac{\Delta V \text{ Output Compensation}}{\Delta V \text{ Current Sense Input}}$$

Characteristics Curve

Figure 1. Timing Resistor versus Oscillator Frequency

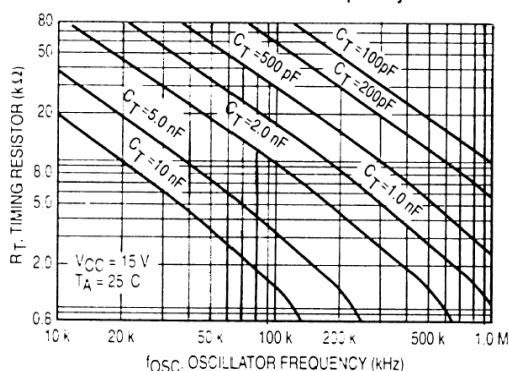


Figure 2. Output Deadtime versus Oscillator Frequency

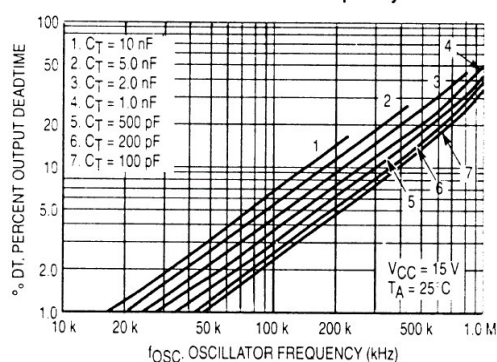


Figure 3. Oscillator Discharge Current versus Temperature

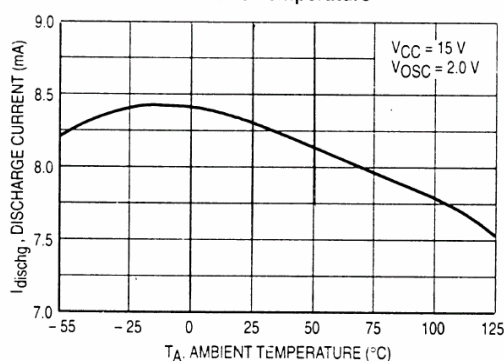


Figure 4. Maximum Output Duty Cycle versus Timing Resistor

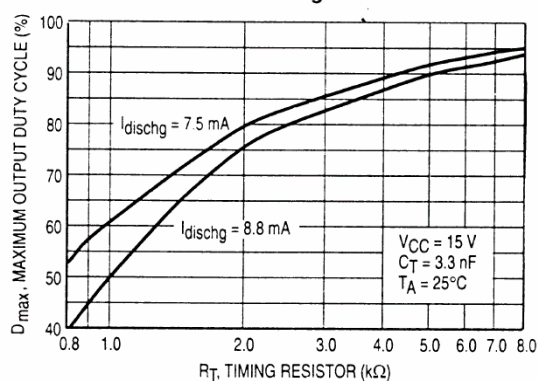


Figure 5. Error Amp Small Signal Transient Response

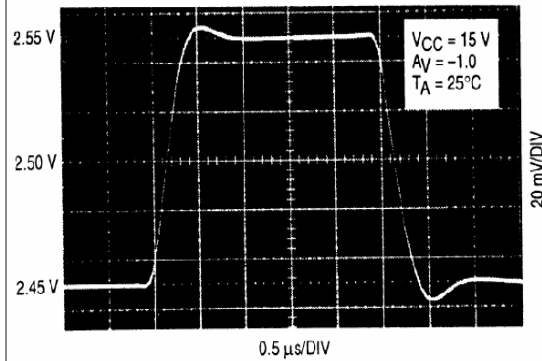


Figure 6. Error Amp Large Signal Transient Response

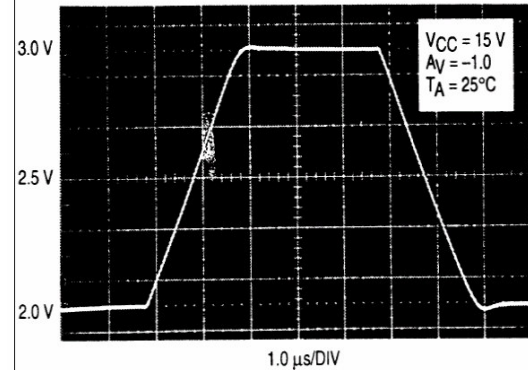


Figure 7. Error Amp Open Loop Gain and Phase versus Frequency

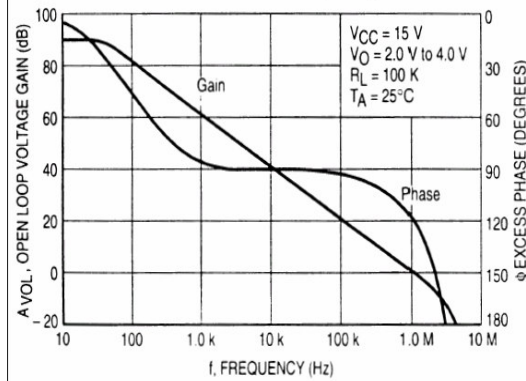


Figure 8. Current Sense Input Threshold versus Error Amp Output Voltage

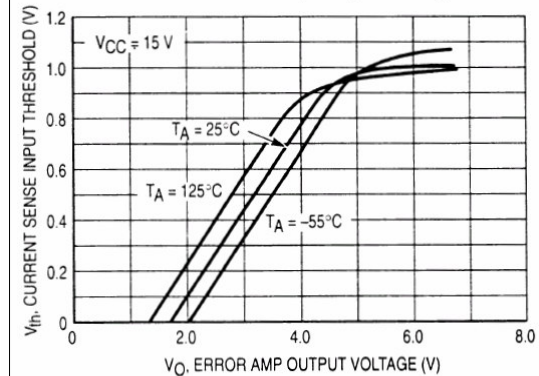


Figure 9. Reference Voltage Change versus Source Current

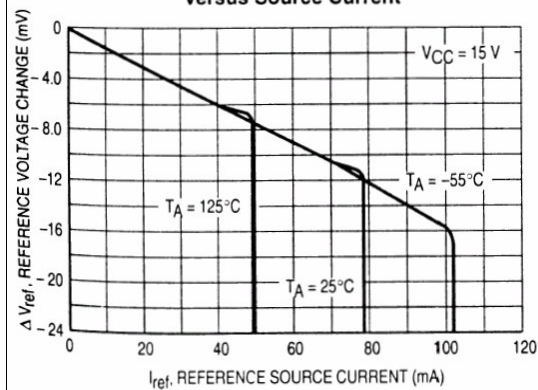
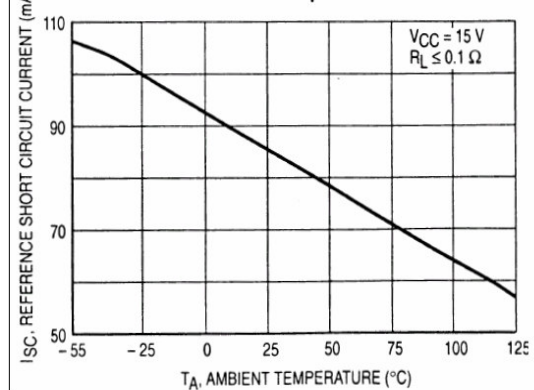
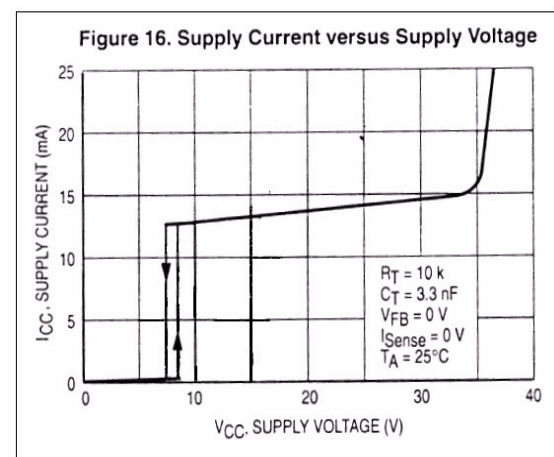
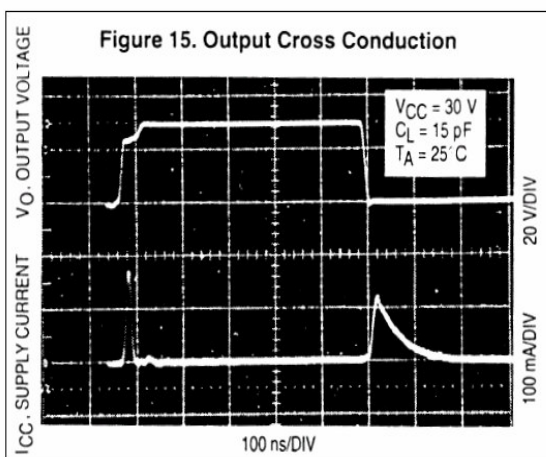
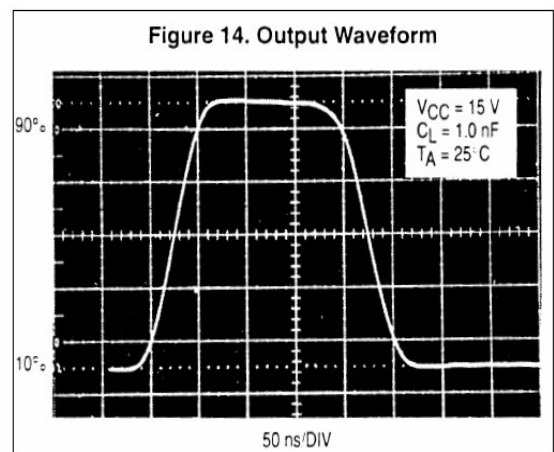
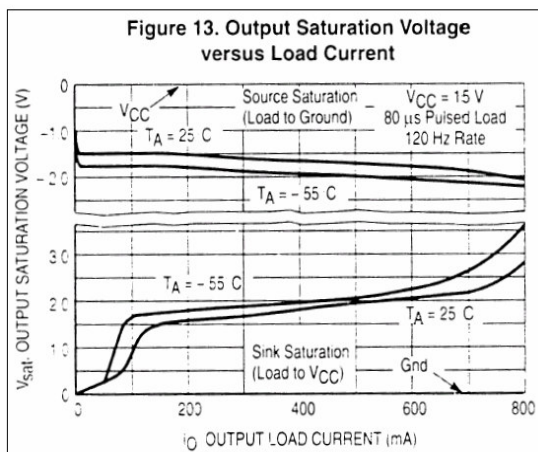
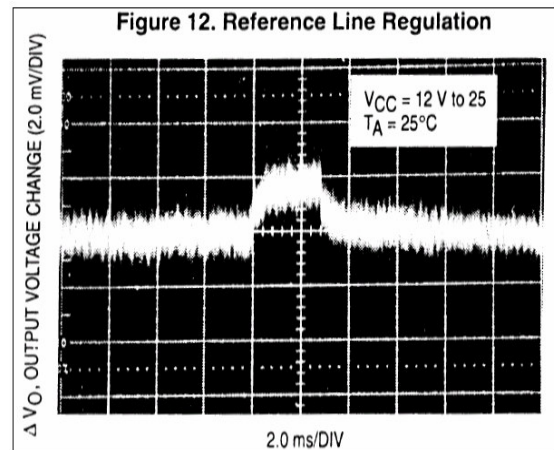
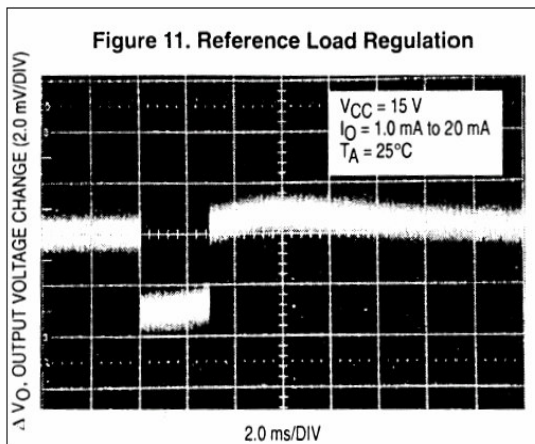


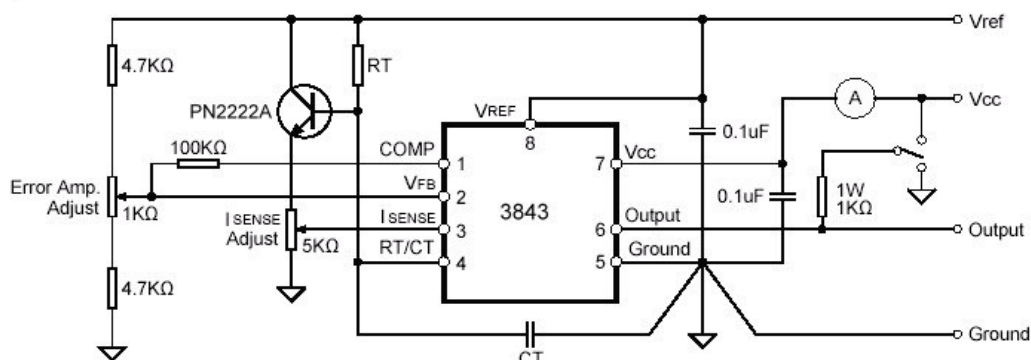
Figure 10. Reference Short Circuit Current versus Temperature





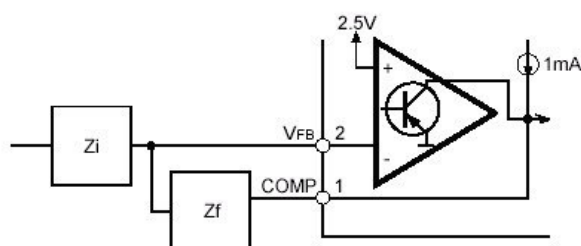
Application Information

Open Loop Test Circuit

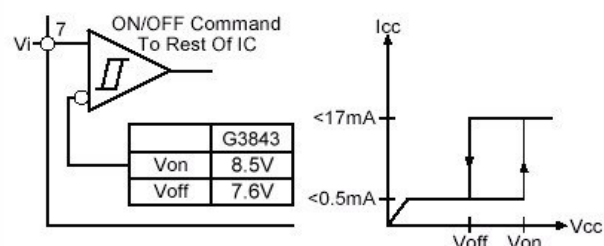


High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin5 in a single point ground. The transistor and 5K Ω potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin3.

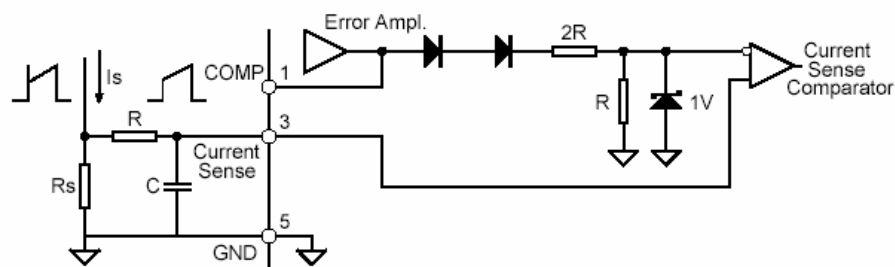
Error Amp Configuration



Under Voltage Lockout

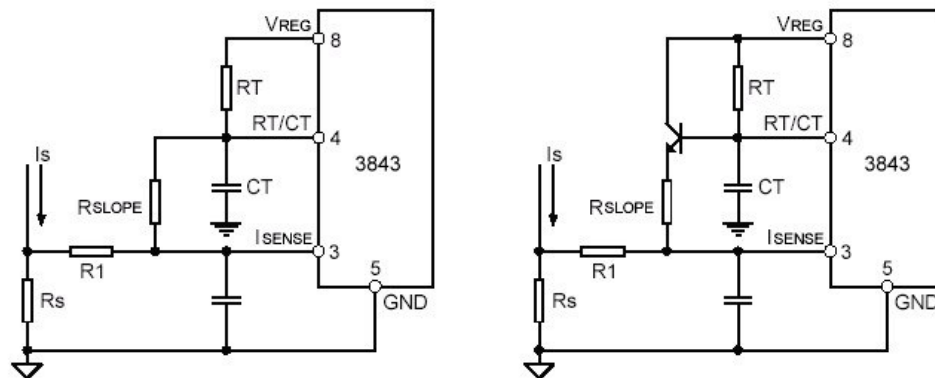


Current Sense Circuit

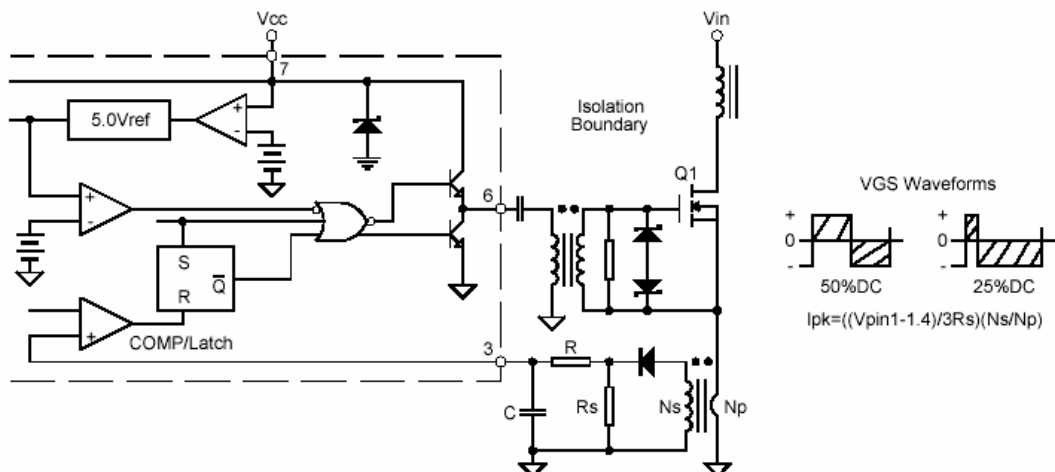


Peak current (I_s) is determined by the formula
 $I_{s(max.)} \approx 1V/R_s$
 A small RC filter may be required to suppress switch transients.

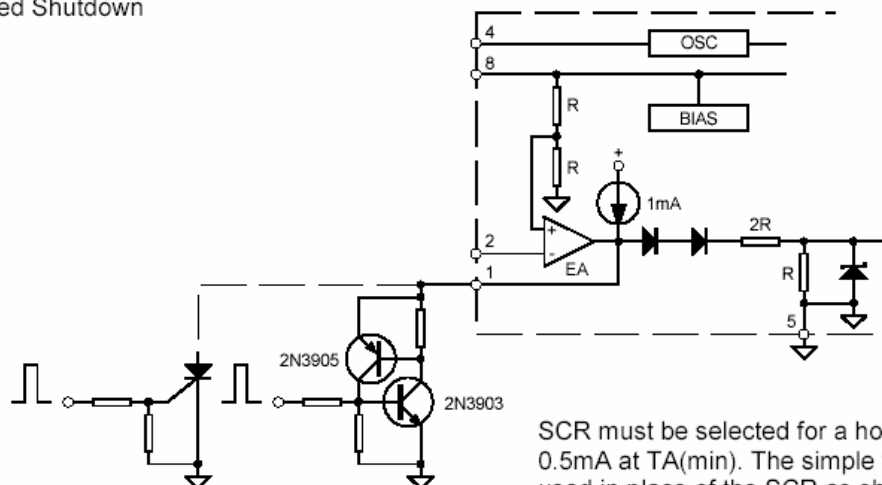
Slope Compensation Techniques



Isolated MOSFET Drive and Current Transformer Sensing

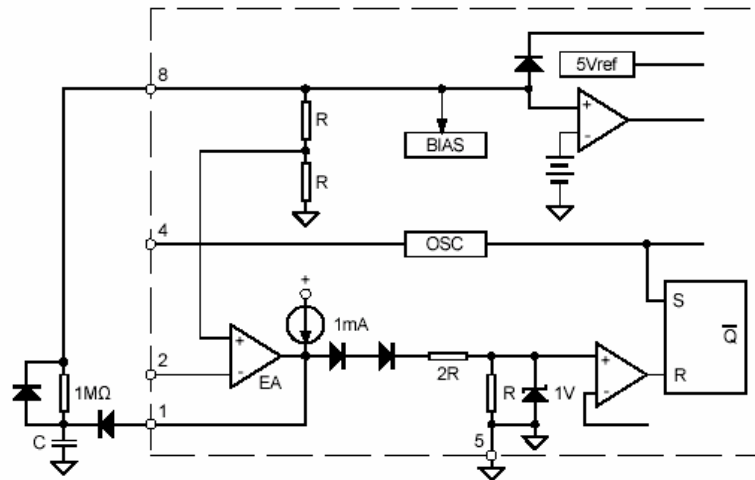


Latched Shutdown

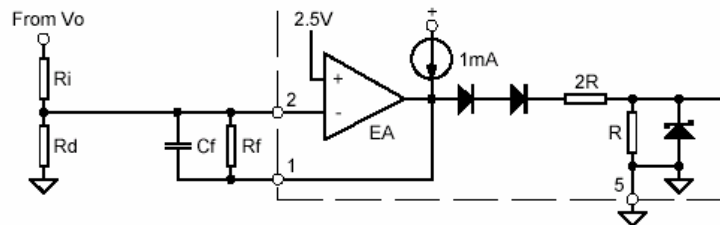


SCR must be selected for a holding current of less than 0.5mA at $T_A(\min)$. The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10K.

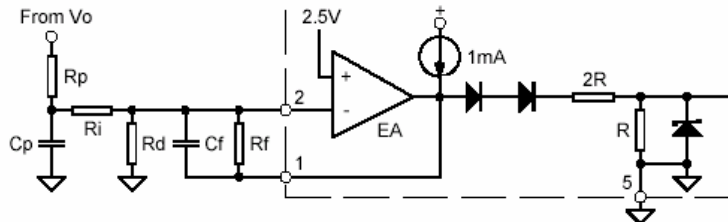
Soft-Start Circuit



Error Amplifier Compensation

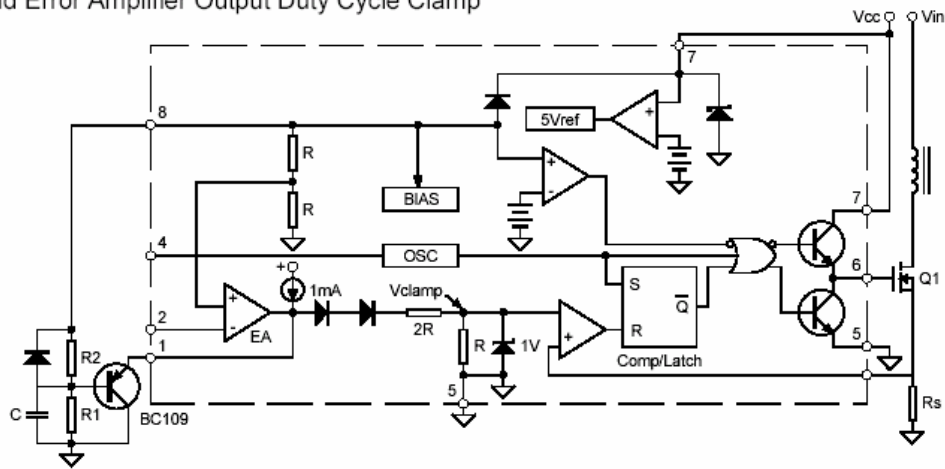


Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current



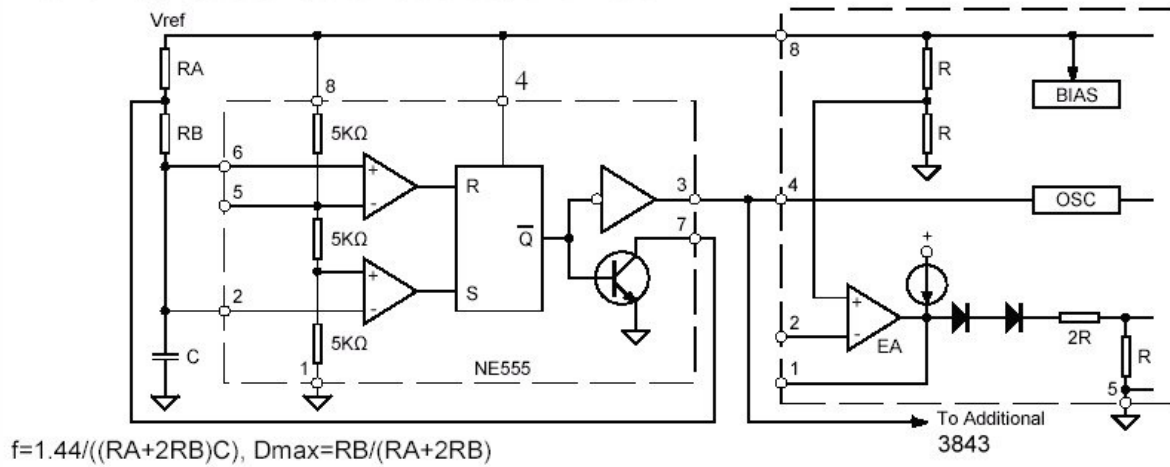
Error Amp compensation circuit for stabilizing current-mode boost and flyback topologies operating with continuous inductor current.

Soft-Start and Error Amplifier Output Duty Cycle Clamp

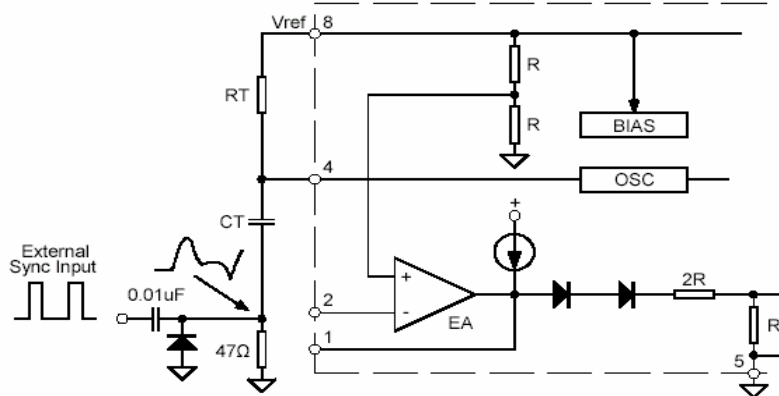


$$V_{\text{clamp}} = R1 / (R1 + R2) \text{ where } 0 < V_{\text{clamp}} < 1V, I_{\text{pk}}(\text{max}) = V_{\text{clamp}} / R_S$$

External Duty Cycle Clamp and Multi Unit Synchronization



External Clock Synchronization



The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of CT to go more than 300mV below ground

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